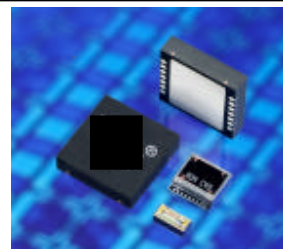


Accelerometers and Inclinometers Digital SPI Output

MSD-H3-2 — Tri-Axis XYZ 2.8V



APPLICATIONS

Drop Detection

Gesture Recognition

Inclination and Tilt Sensing

Image Stabilization

Sports Diagnostics

Vibration Analysis

Static or Dynamic Acceleration

Inertial Navigation and Dead(uctive) Reckoning

Cell Phones and Handheld PDAs

Gaming and Game Controllers

Universal Remote Controls

Theft and Accident Alarms

GPS Recognition Assist

Hard-drive Protection

Pedometers

Computer Peripherals

Cameras and Video Equipment

FEATURES

Ultra-Small Package — 5x5x1.2mm DFN

Precision Tri-axis Orthogonal Alignment

Digital SPI Output

Lead-free Solderability

High Shock Survivability

Excellent Temperature Performance

Low Noise Density

Very Low Power Consumption

Selectable Power Reduction Modes

User Definable Bandwidth

Factory Programmable Offset
and Sensitivity

Self-test Function

PROPRIETARY TECHNOLOGY

These high-performance silicon micromachined linear accelerometers and inclinometers consists of a sensor element and an ASIC packaged in a 5x5x1.2mm Dual Flat No-lead (DFN). The sensor element is fabricated from single-crystal silicon with proprietary Deep Reactive Ion Etching (DRIE) processes, and is protected from the environment by a hermetically-sealed silicon cap wafer at the wafer level.

The D-H3-2 series is designed to provide a high signal-to-noise ratio with excellent performance over temperature. These sensors can accept supply voltages between 2.7V and 5.25V. Sensitivity is factory programmable allowing customization for applications requiring $\pm 1.0g$ to $\pm 6.0g$ ranges. Sensor bandwidth is user-definable.

The sensor element functions on the principle of differential capacitance. Acceleration causes displacement of a silicon structure resulting in a change in capacitance. An ASIC, using a standard CMOS manufacturing process, detects and transforms changes in capacitance into an analog output voltage, which is proportional to acceleration. This voltage is digitized by an on-board A/D converter and is accessed via Serial Peripheral Interface (SPI). The sense element design utilizes common mode cancellation to decrease errors from process variation and environmental stress.

PRODUCT SPECIFICATIONS

PERFORMANCE SPECIFICATIONS ¹			
PARAMETERS	UNITS	MSD-H3-2	CONDITION
Range	g	±2.0	Factory programmable
Sensitivity	mg/count	1.25 typical	
0g Offset vs. Temp.	mg	±150 (x and y) ±300 (z)	Over temp range
	°C	-40 to 85 ²	
Sensitivity vs. Temp	%	±2.0 typical (±3.0 max)	Over temp range
Noise	$\mu\text{g} / \sqrt{\text{Hz}}$	175 typical	
Bandwidth ³	Hz	0 to 3300 max (x and y) 0 to 1700 max (z)	-3dB
Non-Linearity	% of FS	±0.1 typical (±0.5 max)	For 10-90% of range
Ratiometric Error	%	±0.4 typical (±1.5 max)	
Cross-axis Sensitivity	%	±2.0 typical (±3.0 max)	
Resolution	mg	1.25 typical	
A/D Conversion Time ⁴	μs	40 typical	
SPI Communication Speed	MHz	5 typical	
Power Supply	V	2.7 to 5.25	
I/O Pads Supply Voltage	V	1.7 (min) to Vdd (max)	
Current Consumption	mA	0.8 typical	Current draw @ 2.8V
	μA	10 max	Standby—over temperature
ENVIRONMENTAL SPECIFICATIONS			
PARAMETERS	UNITS	MSD-H3-2	CONDITION
Operating Temperature	°C	-40 to 85	Powered
Storage Temperature	°C	-55 to 150	Unpowered
Mechanical Shock	g	4600	Powered or unpowered, 0.5 msec halversine
ESD	V	3000	Human body model
DIGITAL INPUT-PIN SPECIFICATIONS			
PARAMETERS	UNITS	MSD-H3-2	CONDITION
Input Low Voltage	V	$\leq 0.2 * \text{IO Vdd}$	
Input High Voltage	V	$\geq 0.8 * \text{IO Vdd}$	
Input Pull-down Current	μA	60 typical	

Notes

¹ The performance parameters are programmed and tested at 2.8 volts. However, the device can be powered from 2.7 V to 5.25 V. Performance parameters will change with supply voltage variations.

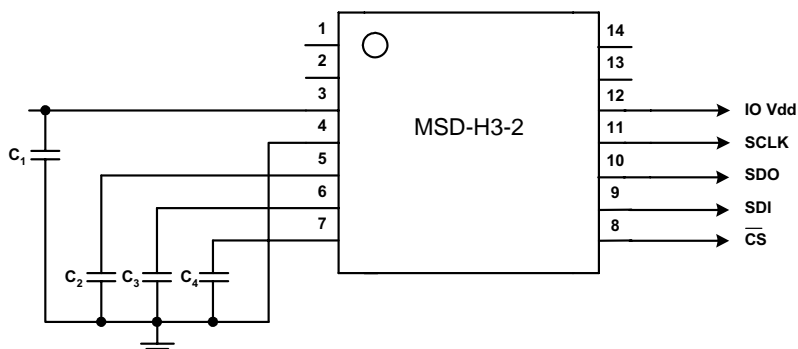
² Temperature range for specified offset.

³ The bandwidth is determined by the external capacitors: C₂, C₃, and C₄ (see application note on page 3).

⁴ A complete conversion and readback of one channel takes approximately 50 μs . This allows all three channels to be repeatedly converted and read at a 6.67KHz rate, well in excess of a typical lowpass filter setting of about 200Hz.

APPLICATION SCHEMATIC & PIN FUNCTION TABLES

Pin	Tri-Axis Function
1	DNC
2	DNC
3	Vdd
4	GND
5	X Output
6	Z Output
7	Y Output
8	CS
9	SDI
10	SDO
11	SCLK
12	IO Vdd
13	DNC
14	DNC



MSD-H3-2 SPI Pin Descriptions

CS – Chip Select SPI enable pin

IO Vdd – Power Supply for I/O pads

SDI – SPI Serial Data Input

SDO – SPI Serial Data Output

SCLK – SPI Communication Clock

GND – Ground

Vdd – Power Supply

X Output – Analog X output low pass filter pin

Y Output – Analog Y output low pass filter pin

Z Output – Analog Z output low pass filter pin

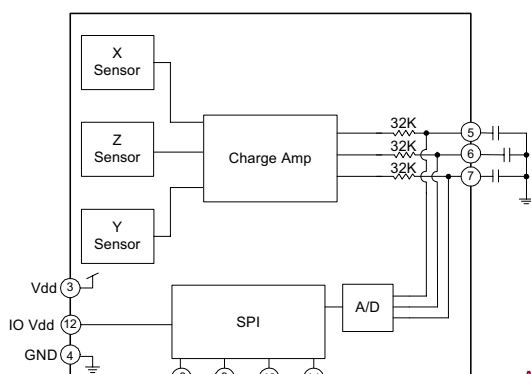
Application Design Equations

The bandwidth is determined by the filter capacitors connected from pins 3, 4 and 5 to ground. The response is single pole. Given a desired bandwidth, f_{BW} , the filter capacitors are determined by:

Notes
$$C_2 = C_3 = C_4 = \frac{4.97 \times 10^{-6}}{f_{BW}}$$

1. Recommend using 0.1 μ F for decoupling capacitor C_1 .
2. Selt test and standby modes are enabled through the SPI interface.
3. X, Y and Z analog outputs are active when the H3-2 is enabled through SPI.

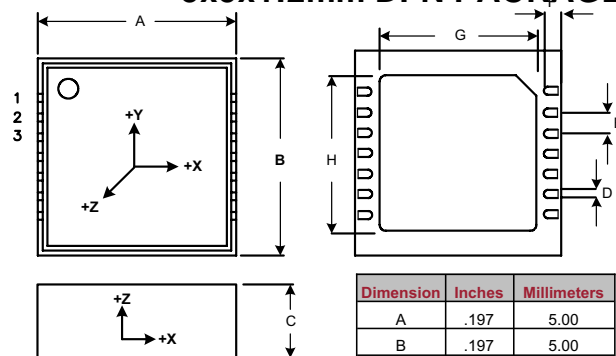
FUNCTIONAL DIAGRAM



Note

1. When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

5x5x1.2mm DFN PACKAGE



Dimension	Inches	Millimeters
A	.197	5.00
B	.197	5.00
C	.047	1.20
D	.009	0.23
E	.020	0.50
F	.016	0.40
G	.142	3.60
H	.142	3.60

ORDERING GUIDE

Product	Axis(es) of Sensitivity	Range (g)	Span (counts)	Sensitivity (mg/count)	Offset (counts)	Operating Voltage (V)	Temperature (°C)	Package
MSD-H3-2	XYZ	2	+/- 1600	1.25	2048	2.8	-40 to +85	5x5x1.2mm DFN

MSD-H3-2 SPI INTERFACE

The D-H3-2 utilizes an onboard Serial Peripheral Interface (SPI) for digital communication. The SPI interface is primarily used for synchronous serial communication between one master device and one or more slave devices. The master, typically a micro controller, provides the SPI clock signal (SCLK) and determines the state of Chip Select (\overline{CS}). The MSD-H3-2 always operates as a slave device during standard master-slave SPI operation.

SPI is a 4-wire synchronous serial interface that uses two control and two data lines. With respect to the Master, the Serial Clock output (SCLK), the Data Output (MOSI) and the Data Input (MISO) are shared among the slave devices. The Master generates an independent Chip Select (\overline{CS}) for each slave device. The slave data output line (SDO) remains in a high-impedance (hi-z) state when the device is not selected, so it does not interfere with any active devices. This allows multiple slave devices to share a master SPI port as shown in Figure 1.

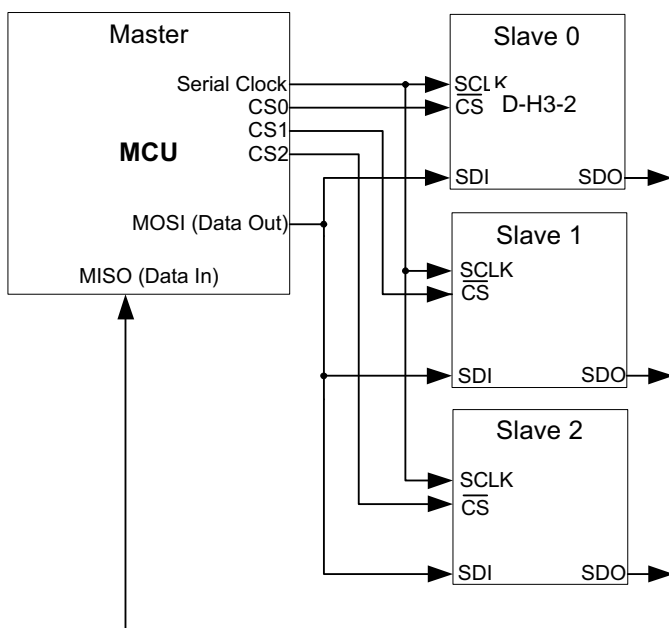


Figure 1 H3-2 SPI Connection

Read and Write Control Registers

The D-H3-2 uses 8-bit read/write commands to communicate with the control register. Upon powering up the D-H3-2 the host (SPI Master) must write to the control register to set the operational mode of the D-H3-2. On the falling edge of \overline{CS} , a 2-byte command is written to the control register. The first byte, 0000 0100, initiates the write and is followed by the user-defined, operational-mode, command byte. This operation occurs over 16 clock cycles. Note that all commands are sent MSB (most significant bit) first, and that the host must return \overline{CS} high for at least 200nS before the next data request. Figure 2 below shows the timing diagram for carrying out the 8-bit control register write operation.

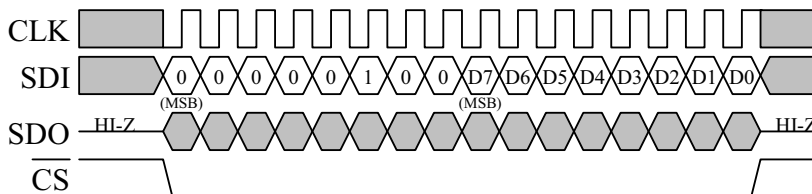


Figure 2 Timing Diagram for 8-Bit Control Register Write Operation

MSD-H3-2 SPI INTERFACE

In order to read the 8-bit control register, the 8-bit read command, 0000 0011, must be written to the slave device to initiate the read. Upon receiving the command, the slave device returns the 8-bit operational-mode data stored in the control register. This operation also occurs over 16 clock cycles. Note that all returned data is sent MSB first, and that the host must return \overline{CS} high for at least 200nS before the next data request. Figure 3 shows the timing diagram for an 8-bit control register read operation.

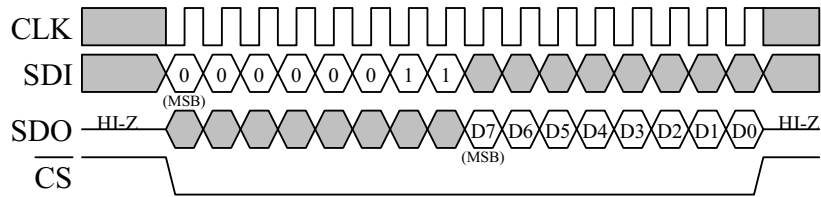


Figure 3 Timing Diagram for 8-Bit Control Register Read Operation

MSD-H3-2 Read Back Operation

The DH3-2 has an onboard 12-bit ADC that can sample, convert and read back sensor data at any time. Transmission of an 8-bit axis-conversion command begins on the falling edge of \overline{CS} . After the eight clock cycles used to send the command, the host must wait for at least 40µS during the ADC conversion time. Note that all returned data is sent MSB first. Once the 12-bit read back data is received, \overline{CS} must be returned high for 200nS before the next data request. Figure 4 shows the timing and register diagrams for the DH3-2 12-bit ADC read operation.

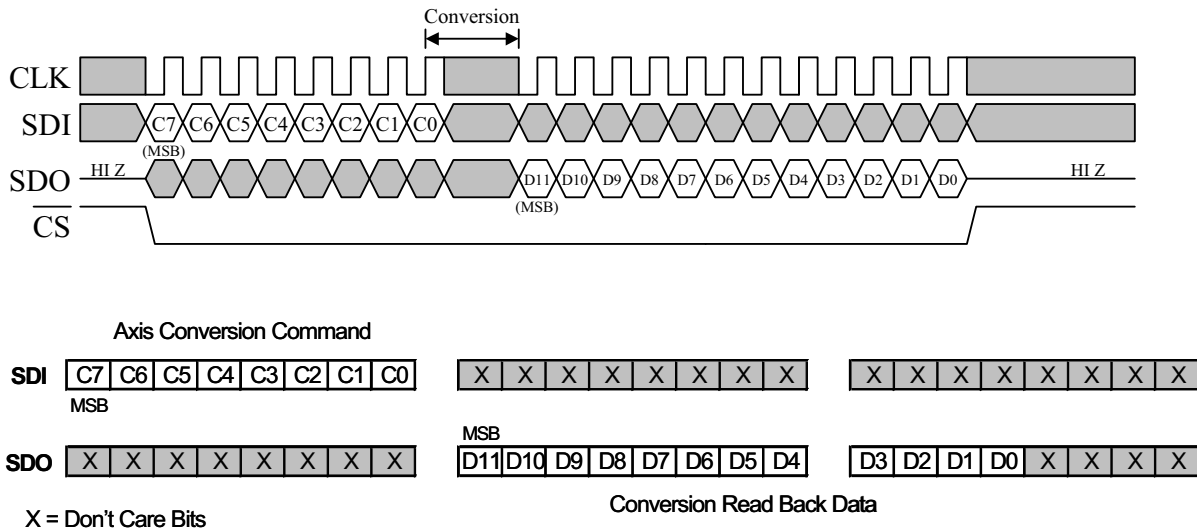


Figure 4 Timing and Register Diagrams for 12-Bit ADC Read Operation

SPI Commands

The DH3-2 SPI interface uses an 8-bit command register to carry out all of its functions. The commands are given in Table 1 on the following page.

MSD-H3-2 SPI INTERFACE

Description	1 st byte (SDI) (Command)
Convert X axis	0x00
Convert Y axis	0x01
Convert Z axis	0x02
Read Control Register	0x03
Write Control Register	0x04

Table 1 Command Register Bit Utilization

Convert X axis (0x00 or 0000 0000) samples the X-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Y axis (0x01 or 0000 0001) samples the Y-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Convert Z axis (0x02 or 0000 0010) samples the Z-axis sensor data held on the filter cap, digitizes it and returns it as 12-bits through SDO.

Read Control Register (0x03 or 0000 0011) reads back the current contents of the control register and returns it as 8-bits through SDO.

Write Control Register (0x04 or 0000 0100) is used to initiate a write to the control register and set the operational mode of the DH3-2. The first byte initiates the write to the register, and the second byte specifies the operational mode.

MSD-H3-2 Operational Modes

The 8-bit read/write control register selects the various operational modes of the DH3-2. Table 2 shows the bit assignments for the available modes.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Speed_0	Speed_1	Enable	Self Test	Parity

Table 2 Read/Write Control Register

Parity reports on even (0) or odd (1) EEPROM parity. A properly functioning part will return even (0) EEPROM parity. This bit is read-only and operates independently of the other modes.

The sampling and power modes controlled by the following bits are detailed below. These bits can be read or written.

Enable powers up the DH3-2 for operation.

Enable = 1 – normal operation - analog outputs also available.

Enable = 0 – low-power standby

Self Test activates the self-test function for the sensor elements on all three axes. A correctly functioning part will increase all channel outputs by approximately 1g when Self Test = 1 and Enable = 1. This bit can be read or written.

Speed_1 is one of two bits used to select the speed/power mode of the DH3-2. See Table 3 on the following page.

Speed_0 is one of two bits used to select the speed/power mode of the DH3-2. See Table 3 on the following page.

MSD-H3-2 SPI INTERFACE

MSD-H3-2 Sample/Power Modes

The DH3-2 ASIC sequentially samples each sensor element in a "round robin" fashion. Note that this is a differential capacitance sampling of each sensor element, which stores an analog value on the filter cap for each axis. In its lowest noise/fastest sample mode, it samples each sensor at 32KHz. This mode also results in the maximum current draw. To reduce system power, four sensor sample rates can be selected in the ASIC control register. See Table 3 below.

Speed_1	Speed_0	Sensor Sample Rate
0	0	32KHz – lowest noise mode
0	1	8KHz
1	0	4KHz
1	1	2KHz – lowest power mode

Table 3 Sensor Sample Rate

MSD-H3-2 SPI Sequence

An example of a SPI sequence for reading sensor data is as follows:

1. Power up H3-2
2. \overline{CS} bar low to select
3. Write operational mode command to 8-bit control register - for example: 0x0404. The first 0x04 is the command to write to the control register and the second 0x04 sets the enable bit in the internal register.
4. \overline{CS} high for at least 200nS (SCLK = 5MHz)
5. \overline{CS} low to select
6. Send convert axis command - for example: 0x000000. The first 0x00 is the command to convert the X-channel. The second and third 0x00 are placeholders. There should be a minimum of 40 μ S between the first and second bytes in order to give the A/D conversion adequate time to complete.
7. The 12-bit A/D data is read in on the second and third SDO bytes.
8. \overline{CS} high for at least 200nS (SCLK = 5MHz)
9. Repeat data read cycle. Recommend reading X-axis, Y-axis, Z-axis, and the Control Register for each read cycle to verify the Control Register mode selection.